Complementary Silicon Power Transistors

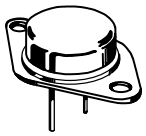
. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4 Adc
- Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

NPN
2N3055*
PNP
MJ2955*

***Motorola Preferred Device**

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
115 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

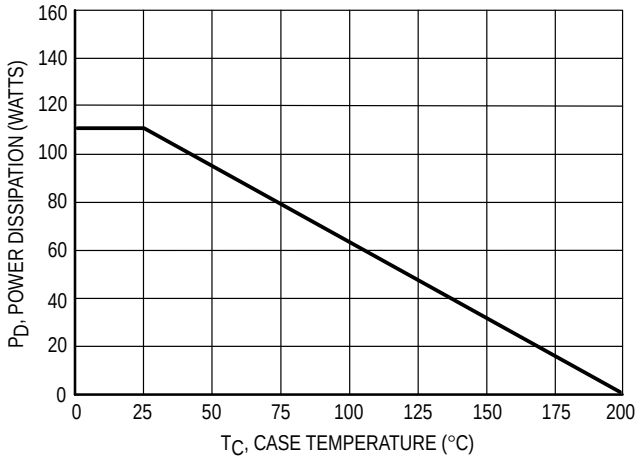


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 —	 1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, Nonrepetitive)	$I_{s/b}$	2.87	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
*Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	—
*Small–Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	—	kHz

* Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

2N3055, MJ2955

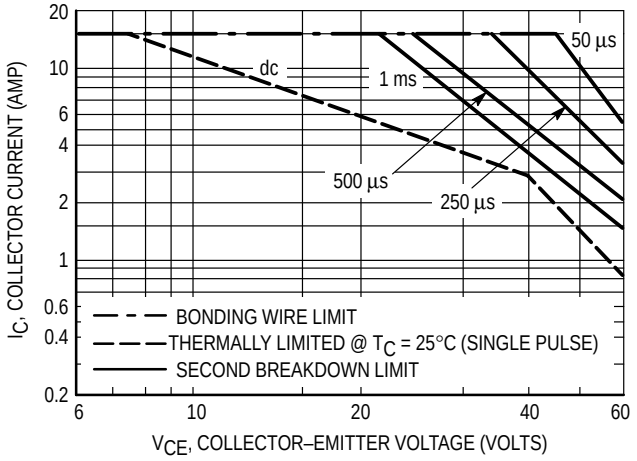
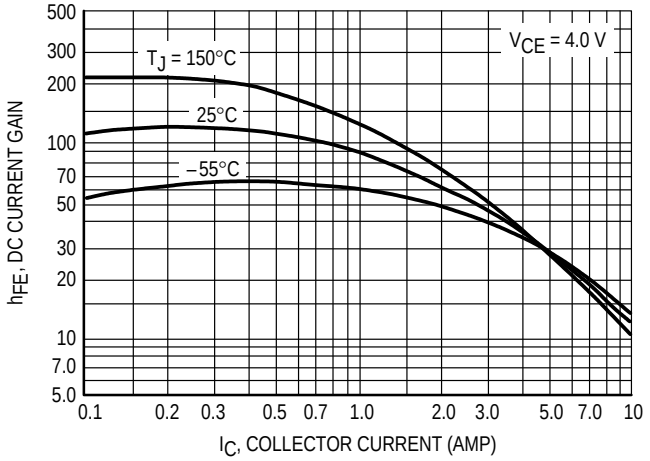


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

NPN
2N3055



PNP
MJ2955

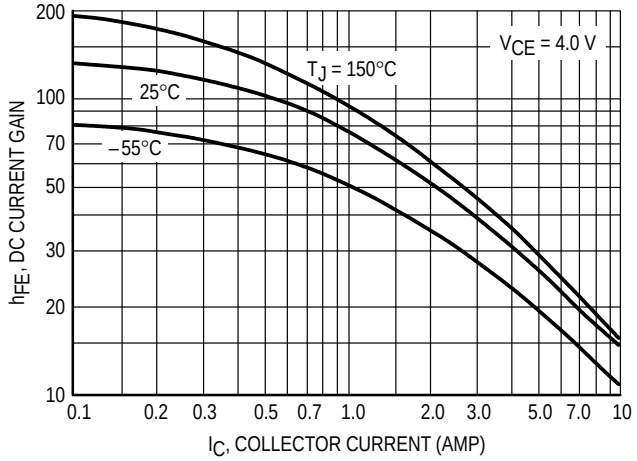
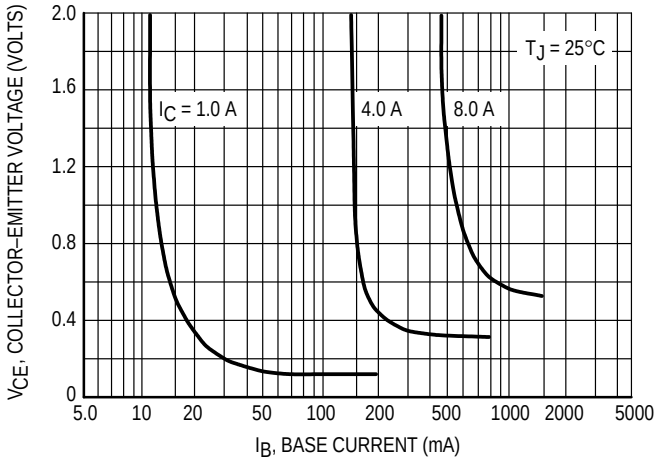


Figure 3. DC Current Gain



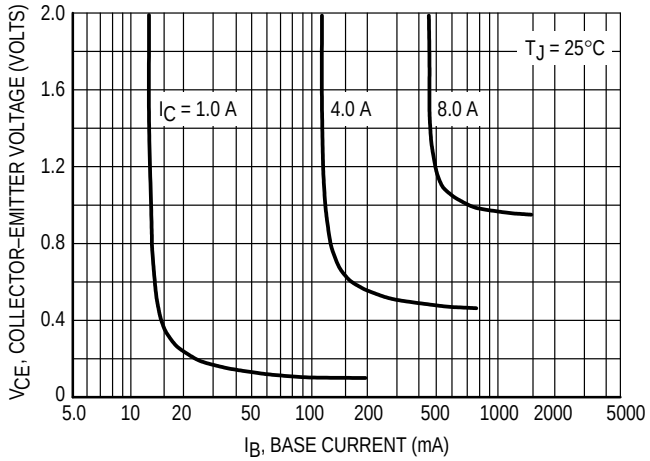
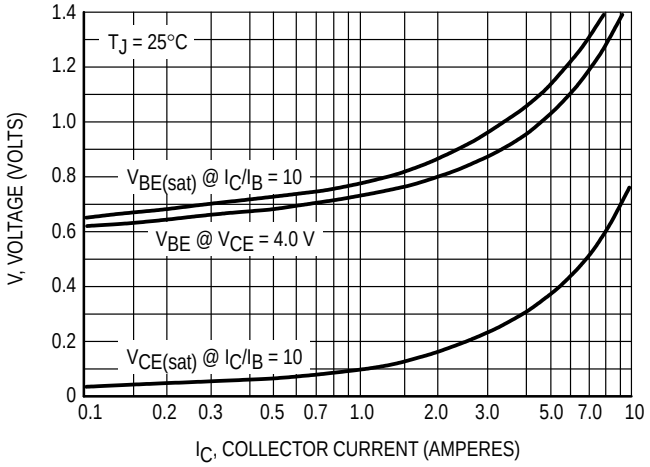


Figure 4. Collector Saturation Region



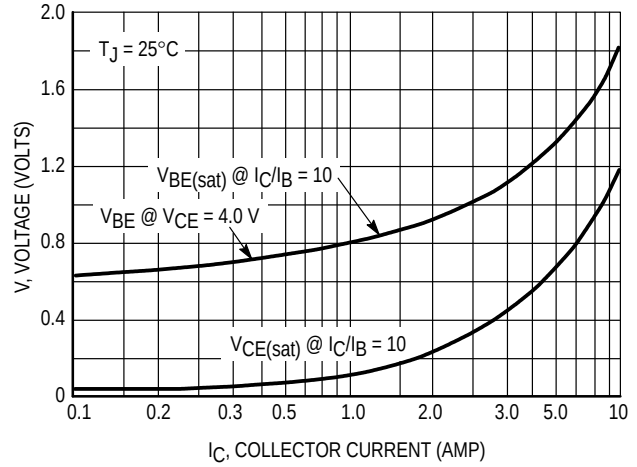
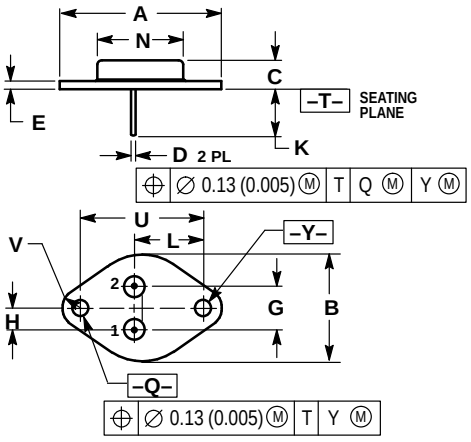


Figure 5. “On” Voltages

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Microsemi LAWRENCE

TECHNICAL DATA

PNP POWER SILICON TRANSISTOR

Qualified per MIL-PRF-19500/514

Devices		*Qualified Level*
2N6274	**2N6277**	**JAN JANTX JANTXV**

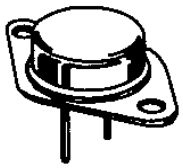
MAXIMUM RATINGS

Ratings	Symbol	2N6274	2N6277	Unit
Collector-Emitter Voltage	V_{CEO}	100	150	Vdc
Collector-Base Voltage	V_{CBO}	120	180	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Base Current	I_B	20		Adc
Collector Current	I_C	50		Adc
Total Power Dissipation @ $T_C = +25^0C$ (1) @ $T_C = +100^0C$ (2)	P_T	250 143		W W
Operating & Storage Junction Temperature Range	T_j, T_{stg}	-65 to +200		^0C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^0C/W$

1) Derate linearly 1.43 W/^{0}C between $T_C = +25^0C$ and $T_C = +200^0C$



TO-3*
(TO-204AA)

*See appendix A for package outline

ELECTRICAL CHARACTERISTICS ($T_C = 25^0C$ unless otherwise noted)

Characteristics		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage I_C = 50 mAdc	2N6274 2N6277	$V_{(BR)CEO}$	100 150		Vdc
Collector-Emitter Cutoff Current V_{CE} = 50 Vdc V_{CE} = 75 Vdc	2N6274 2N6277	I_{CEO}		50 50	µAdc
Collector-Emitter Cutoff Current V_{CE} = 120 Vdc, V_{BE} = -1.5 Vdc V_{CE} = 180 Vdc, V_{BE} = -1.5 Vdc	2N6274 2N6277	I_{CEX}		10 10	µAdc
Emitter-Base Cutoff Current V_{EB} = 6.0 Vdc		I_{EBO}		100	µAdc
Collector-Base Cutoff Current V_{CB} = 120 Vdc V_{CB} = 180 Vdc	2N6274 2N6277	I_{CBO}		10 10	µAdc

ELECTRICAL CHARACTERISTICS (con't)

Characteristics	Symbol	Min.	Max.	Unit
ON CHARACTERISTICS [2]				
Forward-Current Transfer Ratio I_C = 1.0 Adc, V_{CE} = 4.0 Vdc I_C = 20 Adc, V_{CE} = 4.0 Vdc I_C = 50 Adc, V_{CE} = 4.0 Vdc	h_{FE}	 50 30 10	 120	
Collector-Emitter Saturation Voltage I_C = 20 Adc, I_B = 2.0 Adc I_C = 50 Adc, I_B = 10 Adc	$V_{CE(sat)}$		1.0 3.0	Vdc
Base-Emitter Saturation Voltage I_C = 20 Adc, I_B = 2.0 Adc	$V_{BE(sat)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 10 MHz	$\lvert h_{fe} \rvert$	3.0	12	
Output Capacitance V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz	C_{obo}		600	pF
SWITCHING CHARACTERISTICS				
Turn-On Time V_{CC} = 80 Vdc; I_C = 20 Adc; I_B = 2.0 Adc	t_{on}		0.5	µs
Turn-Off Time V_{CC} = 80 Vdc; I_C = 20 Adc; I_{B1} = -I_{B2} = 2.0 Adc	t_{off}		1.05	µs

SAFE OPERATING AREA

DC Tests

T_C = +25^{0}C, 1 Cycle, t = 1.0 s

Test 1

V_{CE} = 5.0 Vdc, I_C = 50 Adc — All Types

Test 2

V_{CE} = 8.6 Vdc, I_C = 165 mAdc — All Types

Test 3

V_{CE} = 80 Vdc, I_C = 29 mAdc — 2N6274

Test 4

V_{CE} = 120 Vdc, I_C = 110 mAdc — 2N6277

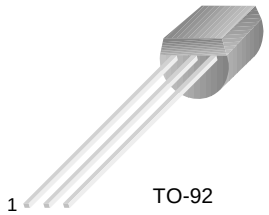
(2) Pulse Test: Pulse Width = 300µs, Duty Cycle ≤ 2.0%.

FAIRCHILD
SEMICONDUCTOR®

BC337/338

Switching and Amplifier Applications

- Suitable for AF-Driver stages and low power output stages
- Complement to BC327/BC328



TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CES}	Collector-Emitter Voltage		
	: BC337	50	V
	: BC338	30	V
V_{CEO}	Collector-Emitter Voltage		
	: BC337	45	V
	: BC338	25	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	800	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

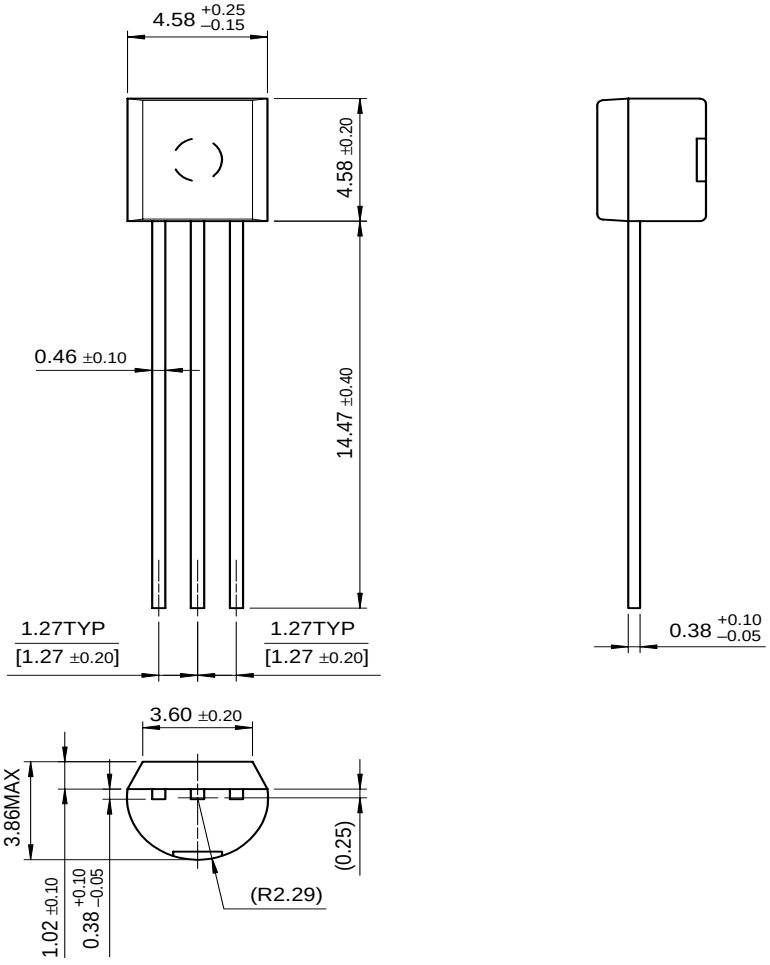
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=10mA, I_B=0				
	: BC337		45			V
	: BC338		25			V
BV_{CES}	Collector-Emitter Breakdown Voltage	I_C=0.1mA, V_{BE}=0				
	: BC337		50			V
	: BC338		30			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=0.1mA, I_C=0	5			V
I_{CES}	Collector Cut-off Current					
	: BC337	V_{CE}=45V, I_B=0		2	100	nA
	: BC338	V_{CE}=25V, I_B=0		2	100	nA
h_{FE1}	DC Current Gain	V_{CE}=1V, I_C=100mA	100		630	
h_{FE2}		V_{CE}=1V, I_C=300mA	60			
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA			0.7	V
V_{BE} (on)	Base Emitter On Voltage	V_{CE}=1V, I_C=300mA			1.2	V
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=50MHz		100		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60-	100-	170-

Package Dimensions

TO-92



Dimensions in Millimeters

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Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E^2CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

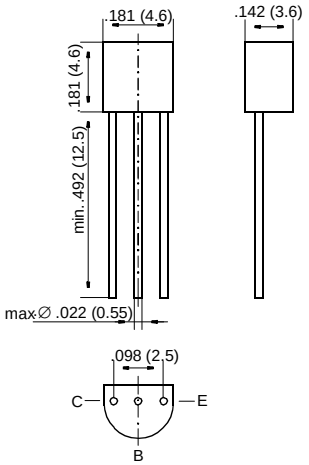
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

BC327, BC328

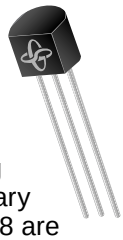
Small Signal Transistors (PNP)

TO-92



Dimensions in inches and (millimeters)

FEATURES



- PNP Silicon Epitaxial Planar Transistors for switching and amplifier applications. Especially suit-able for AF-driver stages and low-power output stages.
- These types are also available subdivided into three groups -16, -25, and -40, according to their DC current gain. As complementary types, the NPN transistors BC337 and BC338 are recommended.
- On special request, these transistors are also manufactured in the pin configuration TO-18.

MECHANICAL DATA

Case: TO-92 Plastic Package
Weight: approx. 0.18 g

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25 °C ambient temperature unless otherwise specified

		Symbol	Value	Unit
Collector-Emitter Voltage	**BC327** **BC328**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector-Emitter Voltage	**BC327** **BC328**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter-Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	800	mA
Peak Collector Current		$-I_{CM}$	1	A
Base Current		$-I_B$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

ELECTRICAL CHARACTERISTICS

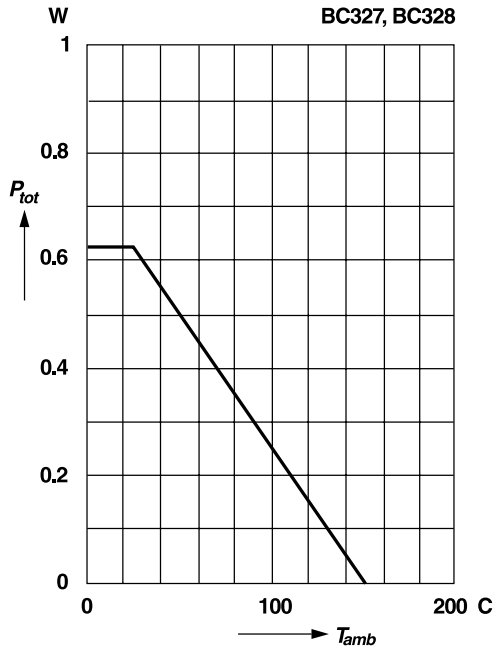
Ratings at 25 °C ambient temperature unless otherwise specified

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA					
Current Gain Group-16	h_{FE}	100	160	250	–
-25	h_{FE}	160	250	400	–
-40	h_{FE}	250	400	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA					
Current Gain Group-16	h_{FE}	60	130	–	–
-25	h_{FE}	100	200	–	–
-40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient Air	R_{thJA}	–	–	200[1)]	K/W
Collector-Emitter Cutoff Current					
at $-V_{CE}$ = 45 V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 25 V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 45 V, T_{amb} = 125 °C **BC327**	$-I_{CES}$	–	–	10	µA
at $-V_{CE}$ = 25 V, T_{amb} = 125 °C **BC328**	$-I_{CES}$	–	–	10	µA
Collector-Emitter Breakdown Voltage at $-I_C$ = 10 mA **BC327**	–	45	–	–	V
BC328	$V_{(BR)CEO}$	25	–	–	V
	–				
	$V_{(BR)CEO}$				
Collector-Emitter Breakdown Voltage at $-I_C$ = 0.1 mA **BC327**	–	50	–	–	V
BC328	$V_{(BR)CES}$	30	–	–	V
	–				
	$V_{(BR)CES}$				
Emitter-Base Breakdown Voltage at $-I_E$ = 0.1 mA	– $V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C$ = 500 mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base-Emitter Voltage at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Gain-Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector-Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF

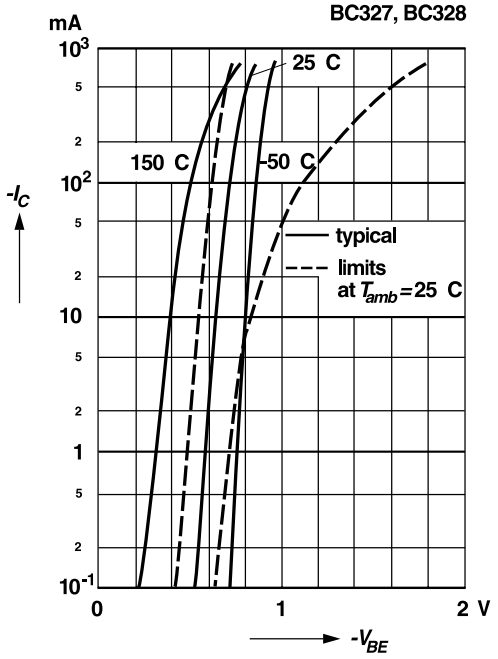
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

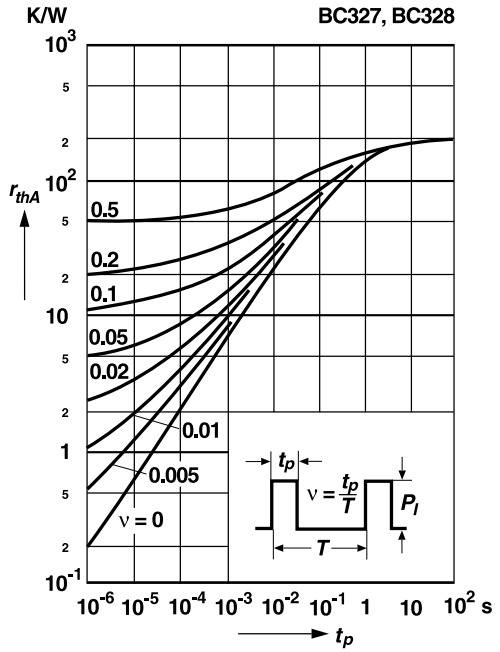


Collector current versus base-emitter voltage

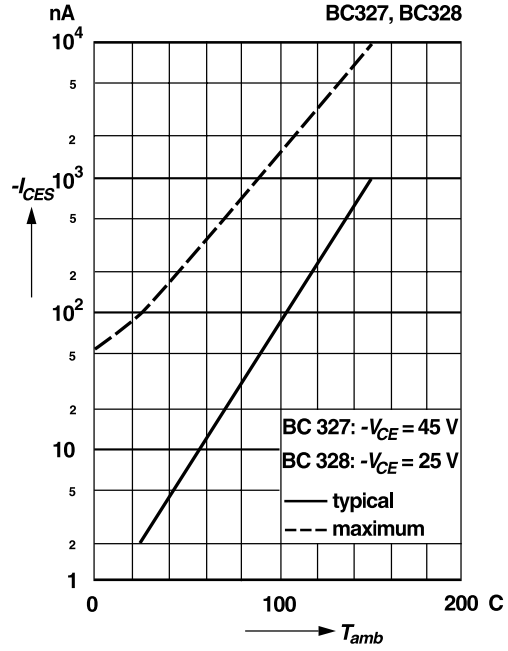


Pulse thermal resistance versus pulse duration

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



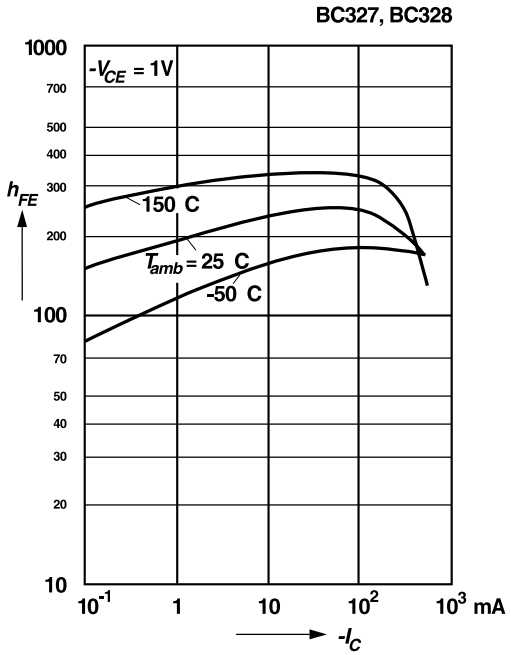
Collector-emitter cutoff current versus ambient temperature



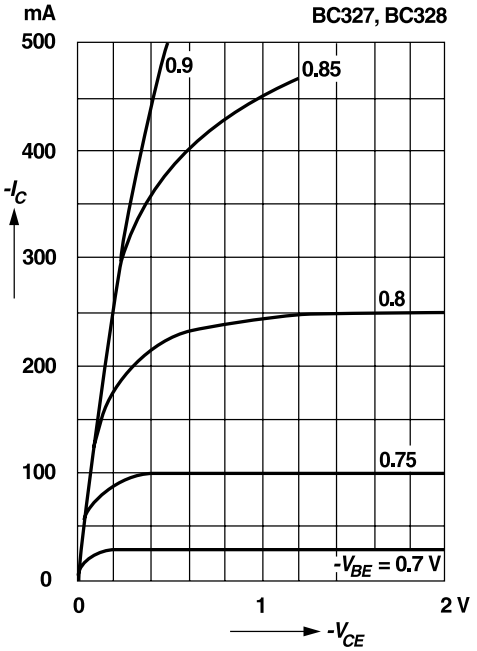
GENERAL SEMICONDUCTOR®

RATINGS AND CHARACTERISTIC CURVES BC327, BC328

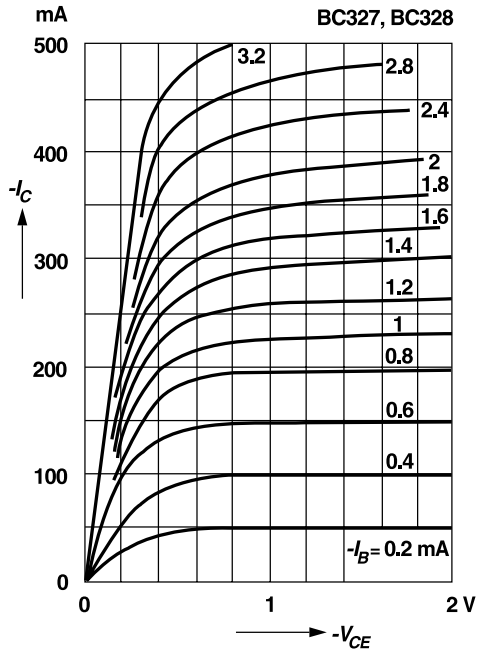
DC current gain
versus collector current



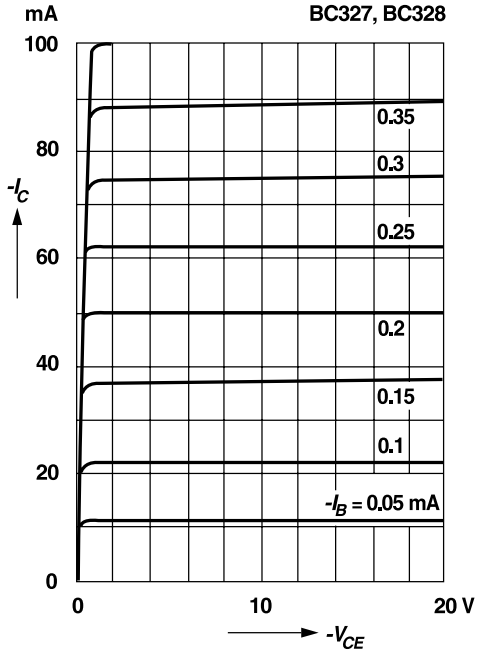
Common emitter
collector characteristics



Common emitter
collector characteristics

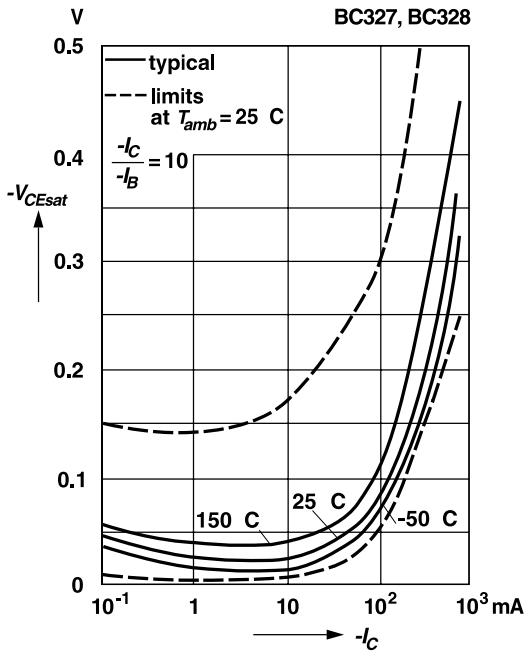


Common emitter
collector characteristics

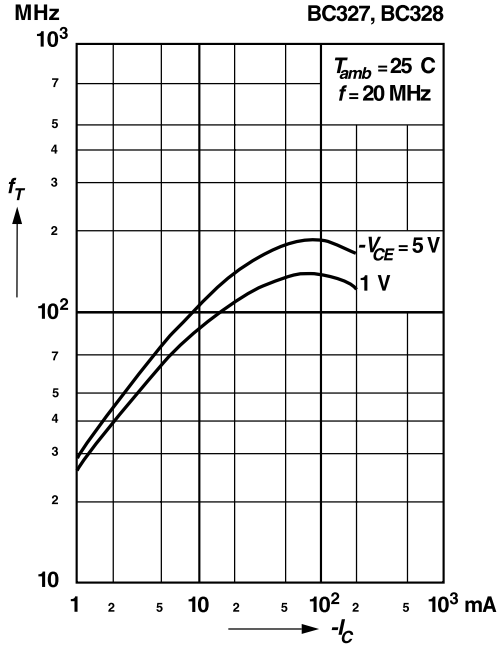


GENERAL SEMICONDUCTOR®

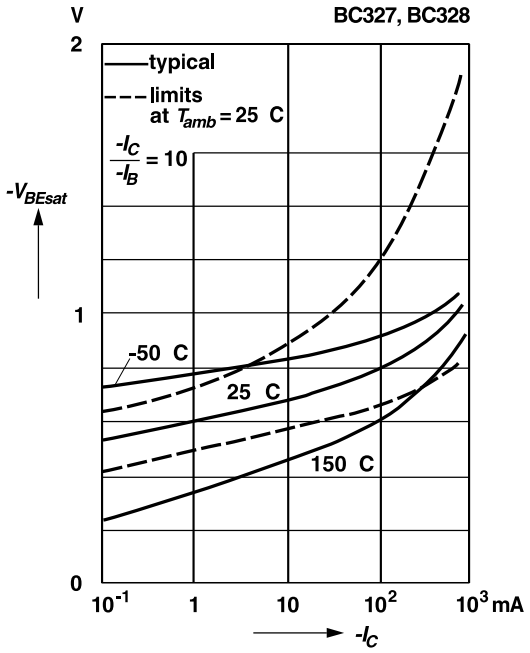
Collector saturation voltage versus collector current



Gain-bandwidth product versus collector current



Base saturation voltage versus collector current



GENERAL SEMICONDUCTOR®

SMPS control circuit SG3524

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

PIN CONFIGURATION

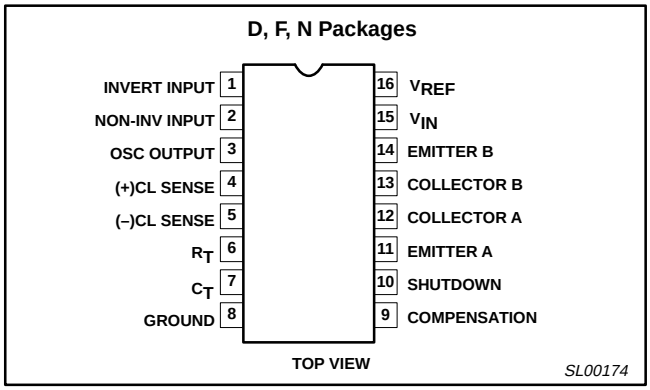


Figure 1. Pin Configuration

FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	SG3524N	SOT38-4
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	SG3524F	0582B
16-Pin Small Outline (SO) Package	0 to +70°C	SG3524D	SOT109-1

BLOCK DIAGRAM

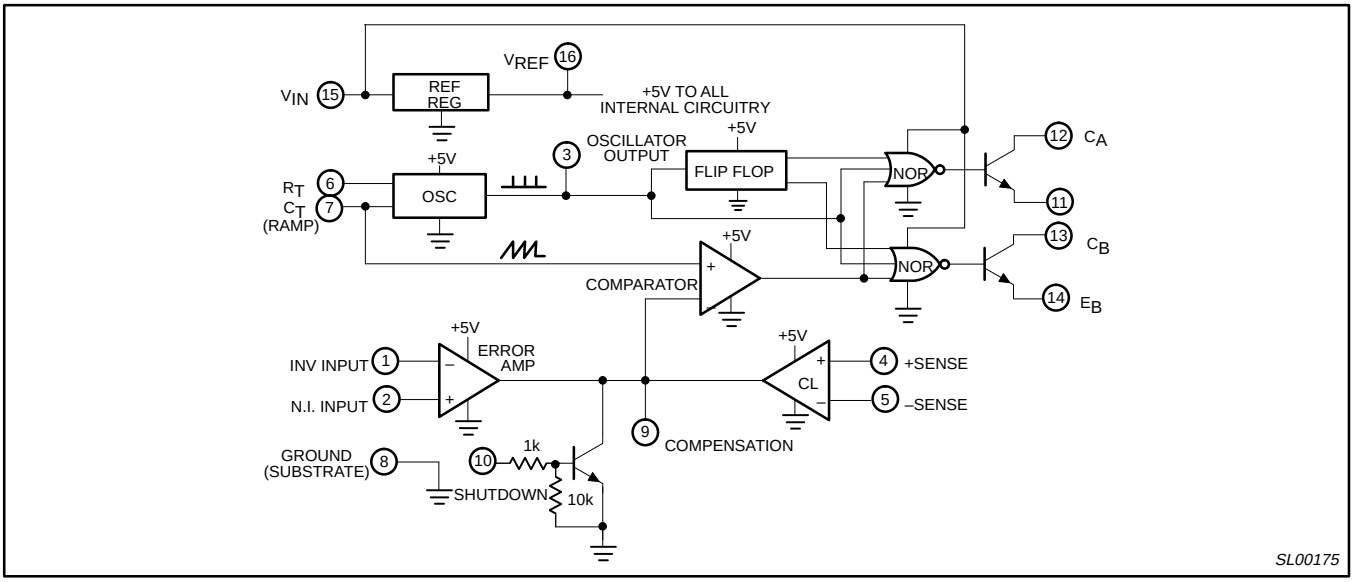


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	40	V
I_{OUT}	Output current (each output)	100	mA
I_{REF}	Reference output current	50	mA
	Oscillator charging current	5	mA
P_D	Power dissipation		
	Package limitation	1000	mW
	Derate above 25°C	8	mW/°C
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

T_A=0°C to +70°C, V_{IN}=20V, and f=20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage		4.6	5.0	5.4	V
	Line regulation	V_{IN}=8 to 40V		10	30	mV
	Load regulation	I_L=0 to 20mA		20	50	mV
	Ripple rejection	f=120Hz, T_A=25°C		66		dB
I_{SC}	Short circuit current limit	V_{REF}=0, T_A=25°C		100		mA
	Temperature stability	Over operating temperature range		0.3	1	%
	Long-term stability	T_A=25°C		20		mV/kHz
Oscillator section						
f_{MAX}	Maximum frequency	C_T=0.001 µF, R_T=2kΩ		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	V_{IN}=8 to 40V, T_A=25°C			1	%
	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, T_A=25°C		3.5		V_P
	Output pulse width	C_T=0.01 µF, T_A=25°C		0.5		µs
Error amplifier section						
V_{OS}	Input offset voltage	V_{CM}=2.5V		2	10	mV
I_{BIAS}	Input bias current	V_{CM}=2.5V		2	10	µA
	Open-loop voltage gain		68	80		dB
V_{CM}	Common-mode voltage	T_A=25°C	1.8		3.4	V
CMRR	Common-mode rejection ratio	T_A=25°C		70		dB
BW	Small-signal bandwidth	A_V=0dB, T_A=25°C		3		MHz
V_{OUT}	Output voltage	T_A=25°C	0.5		3.8	V
Comparator section						
	Duty cycle	% each output “ON”	0		45	%
	Input threshold	Zero duty cycle		1		V
	Input threshold	Maximum duty cycle		3.5		V
I_{BIAS}	Input bias current			1		µA
Current limiting section						
	Sense voltage	Pin 9=2V with error amplifier set for maximum out, T_A=25°C	180	200	220	mV
	Sense voltage T.C.			0.2		mV/°C
V_{CM}	Common-mode voltage		-1		+1	V

DC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 0°C to +70°C, V_{IN} = 20V, and f = 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output section (each output)						
	Collector-emitter voltage (breakdown)		40			V
	Collector-leakage current	V_{CE}=40V		0.1	50	µA
	Saturation voltage	I_C=50mA		1	2	V
	Emitter output voltage	V_{IN}=20V	17	18		V
t_R	Rise time	R_C=2kΩ, T_A=25°C		0.2		µs
t_F	Fall time	R_C=2kΩ, T_A=25°C		0.1		µs
Total standby current						
	(excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN}=40V		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5V output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5V supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0V.

This reference regulator may be used as a 5V source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 3.

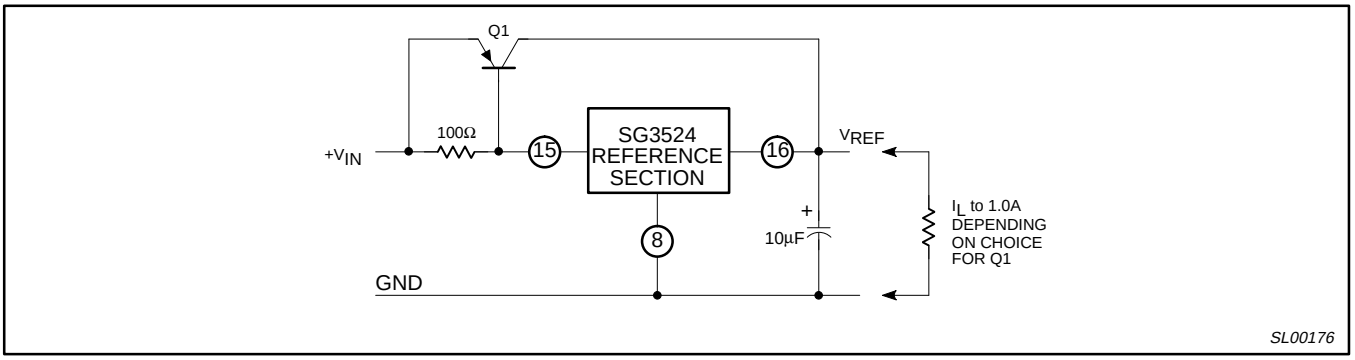


Figure 3. Expanded Reference Current Capability

TEST CIRCUIT

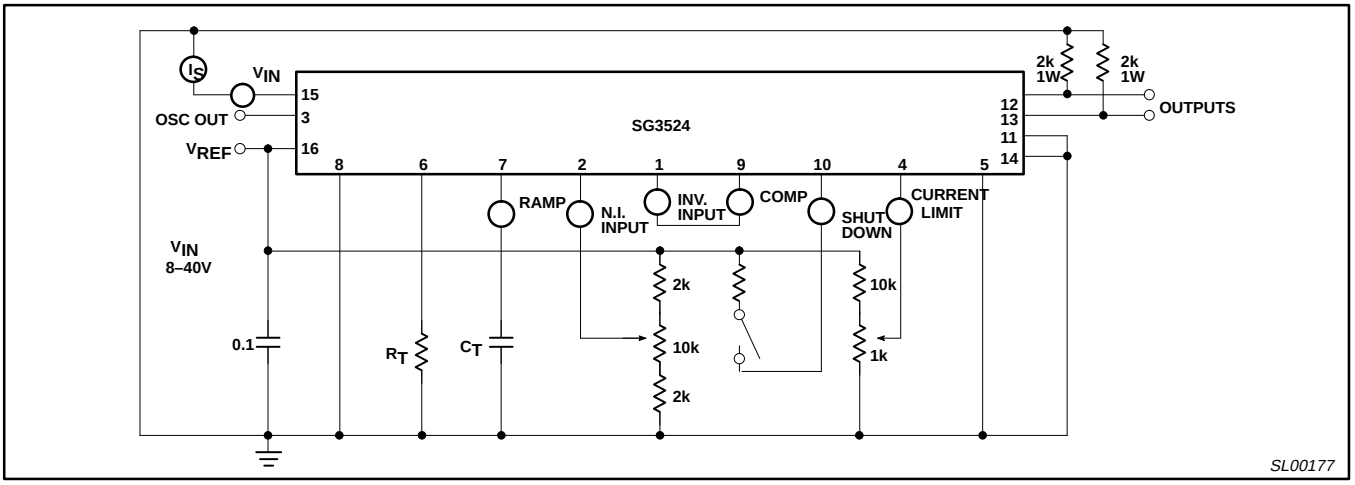


Figure 4. Test Circuit

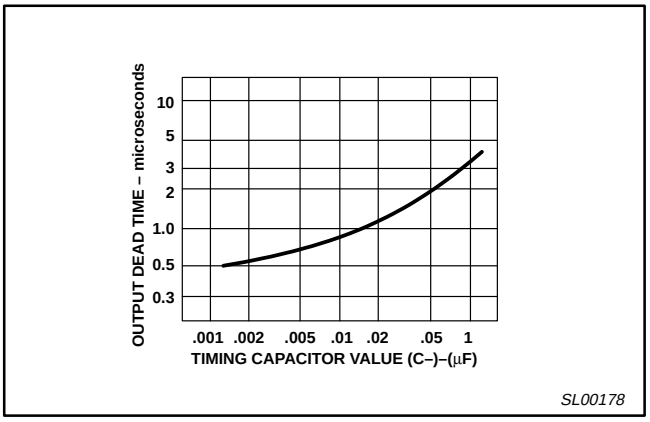


Figure 5. Output Stage Dead Time as a Function of the Timing Capacitor Value

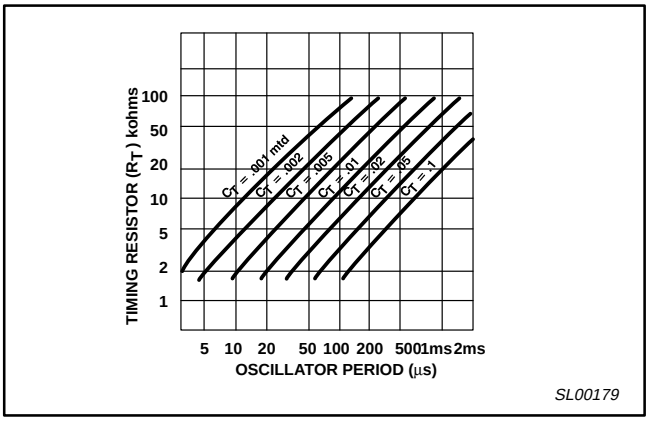


Figure 6. Oscillator Period as a Function of R_T and C_T

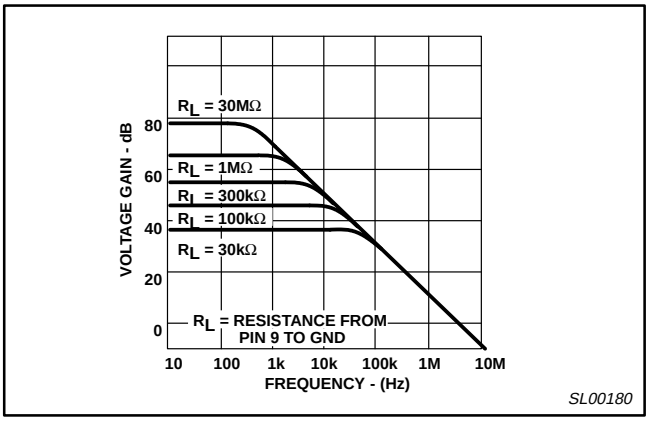


Figure 7. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series-connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6 V ÷ R_T and should be kept within the approximate range of 30μA to 2mA; i.e., 1.8k<R_T<100k.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 5. A pulse width below approximately 0.5μs may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse-width may still be expanded by adding a shunt capacitance (≅100pF) to ground at the oscillator output. [(Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse-width slightly.)] Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.001 and 0.1 μF.

The oscillator period is approximately t=R_TC_T where t is in microseconds when R_T=Ω and C_T=μF. The use of Figure 6 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≅+3V may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse-width apply. The impedance to ground at this point is approximately 2kΩ.

If two or more SG3524s must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T(slave)=one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node (R_L≅ 5MΩ). The gain is

$$A_V = g_M R_L = \frac{8\ I_C\ R_L}{2kT} \approx 0.002R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 7.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 7 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 8. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 9.

By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R_1:

$$\text{Threshold}=V_{BE}(Q1)+I_1R_2-V_{BE}(Q2)$$

$$=I_1R_2 \cong 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1V common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and to shorten an output pulse, should transformer saturation occur. Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal: i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 10. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

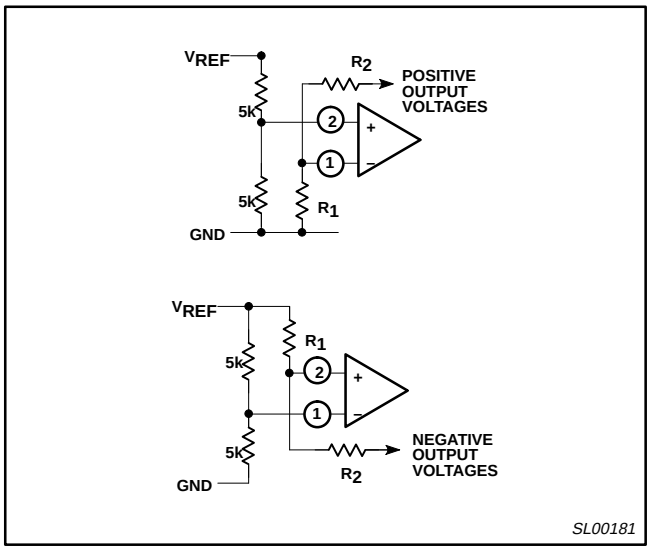


Figure 8. Error Amplifier Biasing Circuits

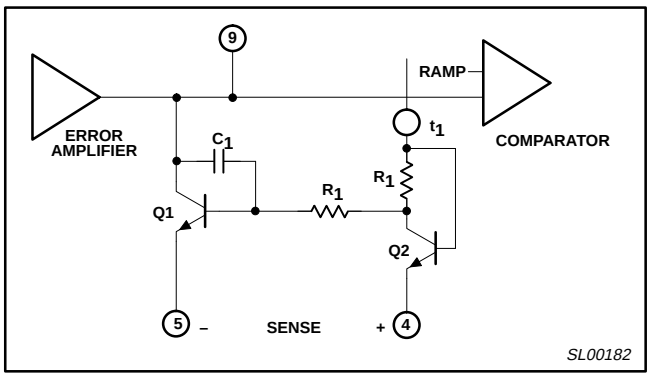


Figure 9. Current Limiting Circuitry of the SG3524

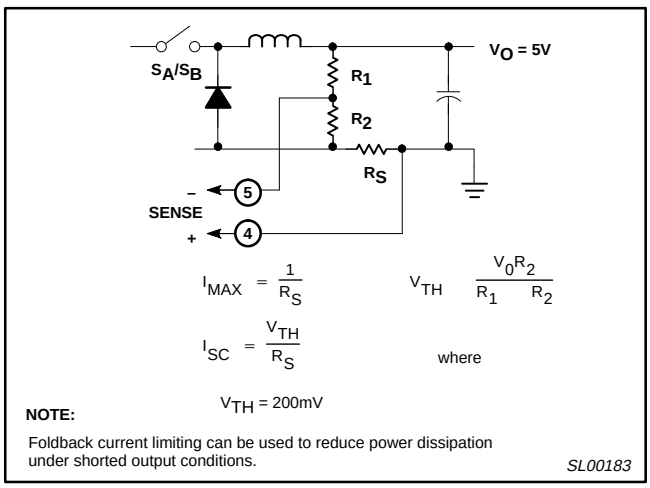


Figure 10. Foldback Current Limiting

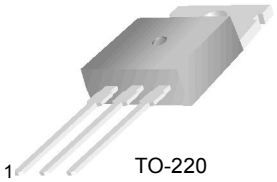
FAIRCHILD SEMICONDUCTOR®

October 2008

TIP120/TIP121/TIP122

NPN Epitaxial Darlington Transistor

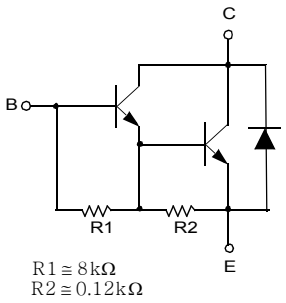
- Medium Power Linear Switching Applications
- Complementary to TIP125/126/127



TO-220

1.Base 2.Collector 3.Emitter

Equivalent Circuit



$R1 \cong 8k\Omega$
$R2 \cong 0.12k\Omega$

Absolute Maximum Ratings* T_a = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage : TIP120 : TIP121 : TIP122	60 80 100	V V V
V_{CEO}	Collector-Emitter Voltage : TIP120 : TIP121 : TIP122	60 80 100	V V V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	5	A
I_{CP}	Collector Current (Pulse)	8	A
I_B	Base Current (DC)	120	mA
P_C	Collector Dissipation (T_a=25°C)	2	W
	Collector Dissipation (T_C=25°C)	65	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 65 ~ 150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Electrical Characteristics* T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage : TIP120 : TIP121 : TIP122	 I_C = 100mA, I_B = 0	 60 80 100			 V V V
I_{CEO}	Collector Cut-off Current : TIP120 : TIP121 : TIP122	 V_{CE} = 30V, I_B = 0 V_{CE} = 40V, I_B = 0 V_{CE} = 50V, I_B = 0			 0.5 0.5 0.5	 mA mA mA
I_{CBO}	Collector Cut-off Current : TIP120 : TIP121 : TIP122	 V_{CB} = 60V, I_E = 0 V_{CB} = 80V, I_E = 0 V_{CB} = 100V, I_E = 0			 0.2 0.2 0.2	 mA mA mA
I_{EBO}	Emitter Cut-off Current	V_{BE} = 5V, I_C = 0			2	mA
h_{FE}	* DC Current Gain	V_{CE} = 3V,I_C = 0.5A V_{CE} = 3V, I_C = 3A	1000 1000			
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = 3A, I_B = 12mA I_C = 5A, I_B = 20mA			2.0 4.0	V V
V_{BE}(on)	* Base-Emitter On Voltage	V_{CE} = 3V, I_C = 3A			2.5	V
C_{ob}	Output Capacitance	V_{CB} = 10V, I_E = 0, f = 0.1MHz			200	pF

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical characteristics

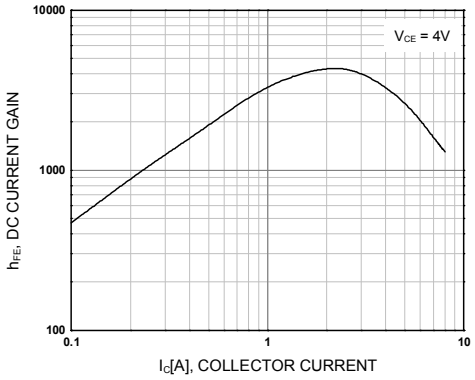


Figure 1. DC current Gain

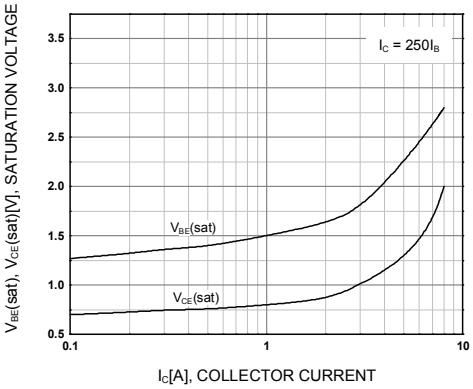


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

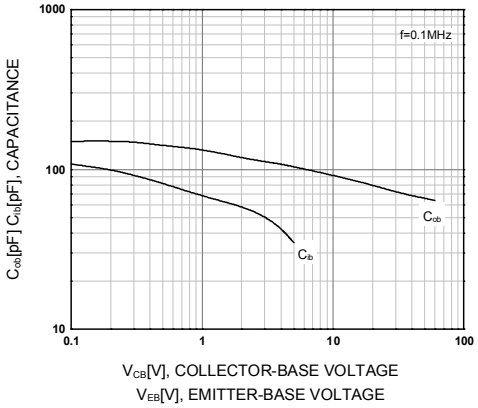


Figure 3. Output and Input Capacitance vs. Reverse Voltage

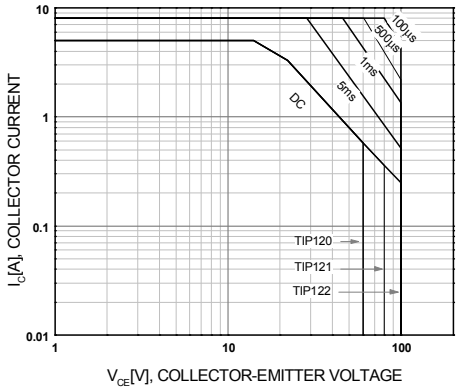


Figure 4. Safe Operating Area

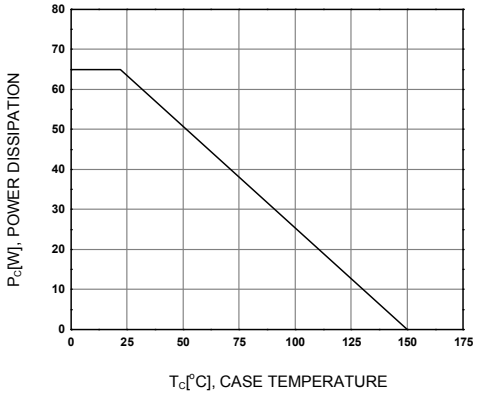
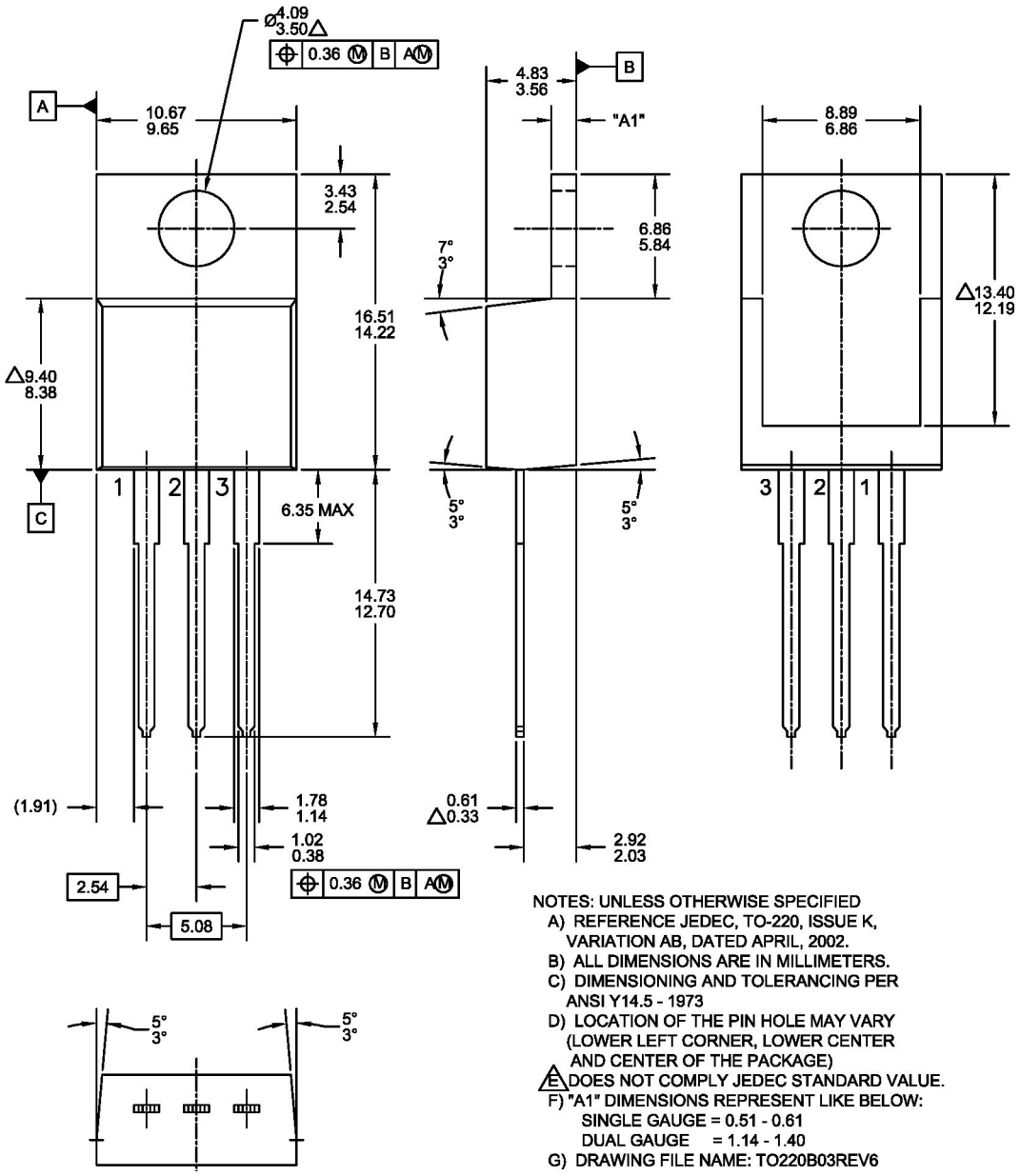


Figure 5. Power Derating

Mechanical Dimensions

TO220



NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973

D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)

△E DOES NOT COMPLY JEDEC STANDARD VALUE.

F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40

G) DRAWING FILE NAME: TO220B03REV6

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Definition of Terms

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